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POWER MANAGEMENT AND DISTRIBUTION FOR SYSTEM ON A CHIP FOR SPACE APPLICATIONS

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ABSTRACT

In this paper a method for achieving integrated power electronics is discussed. Future spacecraft are projected to feature high levels of integration at the system level (i.e., a "systems on a chip" approach) particularly in areas not typically associated with an integrated approach (such as inertial reference systems, RF communications, imaging, sensors, etc.). Taking full advantage of the miniaturization occurring in these other systems will require commensurate reductions in the size of the power electronics. Power electronics are traditionally larger due to the need for high value passive components requiring significant power handling capabilities. Our approach takes advantage of lower projected power requirements and utilizes integrated, on-chip passives and novel high voltage transistors to achieve adaptive distributed on-chip power management and distribution (PMAD). Operating from a single supply, this on-chip PMAD will operate at power levels of up to 1 W, at frequencies of 1-10 MHz.

INTRODUCTION

Integrated systems on future nano-satellites will get their supply voltage from a common power bus. These systems will rely on efficient adaptive on-chip power management circuits for generating the internal voltage levels necessary for operation of the sensors, actuators and other subsystems.

For space applications, there are several challenges in building an efficient completely integrated power management system, including a) the development of a new generation of miniaturized large value passive components (inductors and capacitors) for DC-DC converter circuits that can be integrated on-chip, b) the development of on-chip power interrupt protection (such as microbatteries), c) the development of high voltage transistors that can coexist with traditional low voltage transistors in the same radiation hardened silicon substrate, and d) the development of a library of mixed-signal/mixed-voltage CMOS cells suitable for the construction of a completely integrated on-chip power management system. This paper summarizes JPL's effort in overcoming the challenges of building a completely integrated power management system for future avionics microsystems for deep space applications for NASA.

PMAD REQUIREMENTS FOR AVIONICS SYSTEM ON A CHIP

Figure 1 shows the block diagram of a proposed on-chip adaptive power management system for the next generation of highly miniaturized satellites. Principle components in this on-chip power management system are switching DC-DC converters with large value on-chip inductors and capacitors, micro batteries, battery charge/discharge circuits and digital I/O circuits for interface and control.

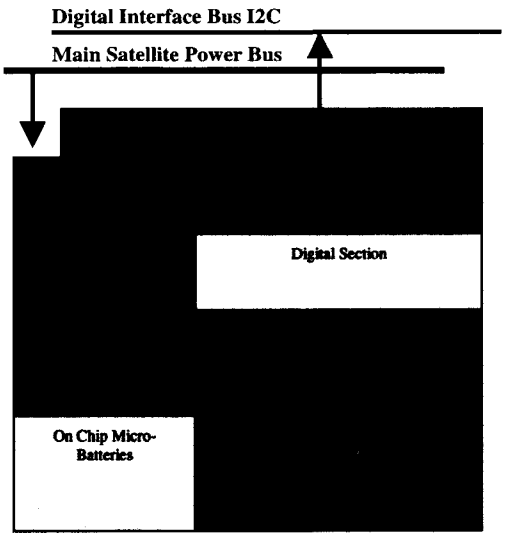

Fig. 1: Next Generation Avionic System On A Chip.

The DC-DC converters translate the voltage of the main power bus to the proper levels for different sections of the chip. In low power avionics system on a chip (SOAC), there may be several on-chip DC-DC converters. Each converter may deliver up to several hundred milliwatts of power to a specific load that is rated at a specific voltage. For example, logic sections of the chip may require 1.8V, while analog mixed-signal sections of the chip may require ±5V [1]. Other areas, such as the vibrating micro-machined sensors and electric motor drive sections, may require 12V to 24V [2]. Efficient voltage conversion is not only achieved through employing switched mode converters but also through adaptively turning each converter on and off on demand.

Adaptive control of the DC-DC converters is accomplished through the digital I/O section that

interfaces with the main flight processor. The flight processor sends signals through a serial interface bus to the I/O section. The I/O section decodes these signals into a corresponding set of instructions for a specific section of the chip and also controls the DC-DC converter powering for that section.

To meet these power demands, the proposed DC-DC converters will employ large value on-chip passives (microhenry inductors and microfarad capacitors). Integration of passive elements with such large values is not currently possible. For example, current integrated spiral inductors produce inductances of only a few nanohenries [3]. To achieve the necessary values for on-chip power applications, an extra layer of ferromagnetic material can be added to the spiral inductors [4].

The integrated PMAD will also employ a bank of micro batteries as an energy storage medium to protect the system against temporary power losses. Thin film based lithium ion micro-batteries utilizing a solid state electrolyte promise to be the front runners for this purpose. A charging/discharge controller section in the PMAD would maintain the battery charge and channel the power from the battery to different on-chip subsystems. It would also monitor the health of the battery and signal battery failure.

For deep space avionic systems, all functions of an integrated PMAD need to be fabricated in a radiation resistant deep sub-micron CMOS process. Silicon on Insulator (SOI) CMOS technology seems to offer the right level of radiation tolerance. However to integrate an avionic PMAD on a chip, we first need to develop a library of SOI CMOS mixed-signal and high-voltage cells. For the SOI mixed-signal library, issues such as the mismatch of transistors, offset between the components, thermal limits, and performance drift due to long term radiation exposure greatly affect the design and need to be considered.

One way to realize the high voltage functional requirements of the library is to use SOI CMOS compatible high voltage transistors. These transistors employ existing lightly doped junctions of the SOI CMOS process for sustaining high voltages. Hence their integration does not burden the SOI CMOS fabrication technology with any additional processing steps. SOI CMOS compatible high voltage transistors are not self aligned and can only withstand the higher voltage on their drain terminal. As a result design of high voltage functions using these transistors requires the development of new innovative circuit topologies that can tolerate these inherent limitations.

PASSIVE COMPONENTS FOR ON-CHIP DC-DC CONVERTERS

DC-DC converters play a critical role in adaptive integrated PMAD for space applications. Of the various power electronics subsystems, however, DC-DC converters are the most difficult to miniaturize and integrate due to a reliance on high value passive components, namely the energy storing inductive and capacitive elements.

Moving away from typical surface mount technologies and towards integrated passives would not only reduce mass and volume, but could enhance reliability and performance, as well as make adaptive, distributed power easier to implement.

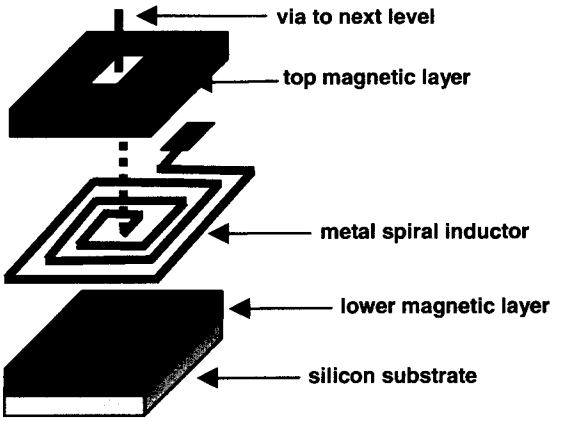

Fig. 2: Schematic of an on-chip microinductor incorporating magnetic films.

On-chip inductive elements are a particular challenge to integrate due to the need for magnetics. Current on-chip inductors used in microwave and rf applications typically consist of a spiral patterned from an existing metallization layer [3]. These components, however, possess insufficient inductances per unit area and quality for efficient power conversion. One approach to circumvent these limitations in quality and power handling capabilities in the 1-10 MHz range is to add thick magnetic materials which enhance the energy storage capacity and inductance (Fig. 2), making viable an integrated, monolithic approach to DC-DC converters.

To implement such an approach requires a careful consideration of many design factors. First, numerous parasitics, including those between the spiral lines, between the substrate and spiral, and between the spiral and magnetic material, limit performance over a given frequency range. Also critical is the choice of materials, which must enhance inductance per unit area as well as handle

power densities higher than 1 W/mm^2. Finally, critical related issues such as EMI and thermal stability of the magnetic material must be considered.

Due to the need for energy storage, relatively large volumes of magnetic material are needed, necessitating thick (>1 μm) magnetic films. Two proposed core materials are Ni-Fe based permalloy [5] and CoZr based amorphous alloys [4]. Although CoZr may potentially posses a high saturation magnetization (determined by the exact content of Zr) and therefore higher power handling capabilities, it is not readily electrodeposited, and is typically deposited by sputtering. Permalloy is the prototypical soft magnetic material, optimized by years of industrial application, most notably in read-write head applications. Fortunately, these materials are amenable to electroplating, allowing patterning of the component on-chip using thick photolithography techniques. Electrodeposition is a particularly attractive method, not only due to the low cost and ease of use, but due to its inclusion in industry roadmaps which project utilizing electrodeposition for copper metallizations. The most significant problems which must be addressed include adhesion and stress issues, related to the use of thick magnetic films, as well as the need for diffusion barriers to prevent fast diffusers such as Fe from migrating into dielectrics where they reduce breakdown, and into silicon where they form deep level traps.

Since magnetic materials are not available within standard CMOS processing lines, the magnetic material must be added after fabrication of the high voltage transistors, requiring a post processing step.

Integrated spiral inductors contain many parasitic elements that change the effective inductance and resistance. In inductors without magnetic materials ("air coils") these can be modeled to first order by frequency-independent, linear lumped elements. These elements include:

- capacitors that model displacement currents in the isolating dielectric and the dielectric or semiconducting substrate
- coupled inductors that model voltages induced in neighboring windings and other metallic or semi-metallic layers
- resistors that model conduction currents impressed or induced in metallic or semi-metallic layers.

To illustrate the complexity of the parasitic effects in Fig. 3 the lumped-element circuit used for a spiral inductor over a gold layer on a silicon substrate is shown. This circuit is valid for frequencies up to 300 MHz. The circuit for the integrated inductor can be directly inserted into SPICE-type circuit models and analyzed together with lumped elements for the storage capacitor and the switching transistors.

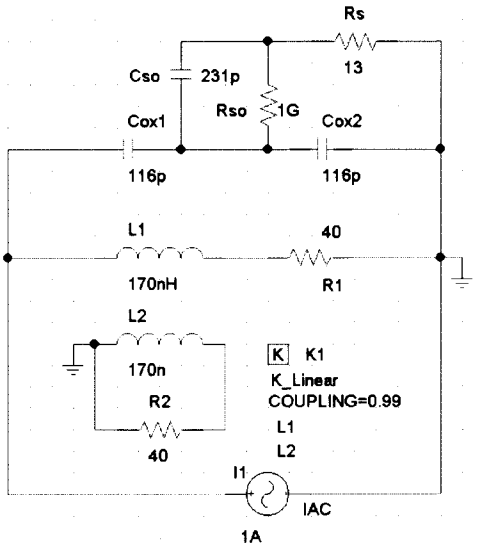

Fig. 3: Inductor circuit model with frequency-independent lumped elements. L2 and R2 model the eddy currents in a gold layer. The elements added in the upper portion model the insulator and silicon substrate.

It is the goal of our modeling effort to eventually develop lumped circuit elements for inductors with magnetic layers. Analytical solutions are available only for conducting rings over planar magnetic layers, which are not optimal for flux closure. We are exploring more realistic structures with a commercial finite-element-analysis package, which solves the complete Maxwell equations, thus including eddy current, skin, and proximity effects. The package also provides a thermal analysis.

Large value capacitors also present a challenge in the context of on-chip PMAD. To maintain sufficient breakdown voltages while providing sufficient capacitances requires the consideration of high dielectric materials. As gate oxide thickness utilizing silicon dioxide ($k\approx4$) reach their useful limit, other materials such as tantalum oxide ($k\approx425$) and even ferroelectric materials ($k\approx10^3$-10^4) provide a means to achieving the necessary capacitances on-chip. These materials also offer added degrees of freedom in terms of controlling the breakdown voltage and radiation hardness. Processing and fabrication of these materials presents the most significant challenge, which may include using low-

temperature electrochemical techniques such as anodization [6].

ON-CHIP LITHIUM AND LITHIUM ION THIN FILM, RECHARGEABLE BATTERY TECHNOLOGY

Projected lower power levels for future micro/nanospacecraft make possible the use of thin-film solid state microbatteries as possible back-up power sources for on-chip PMAD. It is therefore of high technological interest to develop long lasting, high specific energy thin-film batteries that can be used as an integral part of the microelectronic circuit. The advantages offered by thin-film microbatteries for on-chip power applications include : 1) manufacturing techniques similar to those used for microelectronics devices, enabling integration with the electronic circuit board, 2) the use of an extremely thin electrolyte layer of relatively poor conducting ionic conductors such as glassy solid electrolytes and 3) the ability to construct the microbattery in any desired two-dimensional shape. Such microbatteries are expected to provide localized low-power supports for voltage reference and maintenance as well as memory protection. They replace those capacitors that are commonly used external to the microelectronic device. The substitution of the capacitors with microbatteries as a backup power unit will not only offer significant advantages in terms of weight and volume (batteries have ~20 times the specific energy compared to capacitors) but also pave way for advanced memory storage devices such as self-powered CMOS memories and RAMs.

The lithium based battery is recognized as the most viable rechargeable battery system, due to the highest oxidation potential of Li and lowest equivalent weight. Accordingly, Li batteries have voltages as high as 4 V when combined with several transition metal chalcogenide cathodes that undergo reversible intercalation reactions with lithium. For the cathode material, the transition metal chalcogenides with either two-dimensional layered structure or a three dimensional framework tunnel structure, forming van-der-Waals bonded compounds with lithium are useful [7]. Typical cathode materials include molybdenum oxide [8], titanium disulfide [9,10] and vanadium oxide [11,12,13]. The use of carbonaceous materials and tin oxides as alternate anode materials to metallic lithium has contributed to an improvement in the cycle life, safety and reliability, albeit with reduced cell voltages and specific energies. To partly offset the latter, high voltage (> 4V) cathodes such as lithium cobalt oxide, lithium nickel-cobalt oxide and lithium spinel manganese oxide ($LiMn_2O_4$) [14-17] are being used in lithium ion cells. All these materials are characterized by high specific energy of over 500 Wh/kg (against Li) and high diffusivity for lithium (10^{-12} to 10^{-8} cm^2/s) in the lattice to permit high current discharges of the microbatteries. The solid electrolytes for the lithium solid state batteries are generally mixtures of oxides/sulfides of phosphorous, silicon, germanium and bismuth with high lithium ion conductivity (10^{-6} to 10^{-4} S/cm at 25^0 C), and negligible electronic conductivity (< 10^{-13} S/cm) to prevent self-discharge of microbattery. Significant developments on the thin-film battery have been made mainly at three laboratories, i.e., Eveready Battery Co., Oak Ridge National Laboratory and Bellcore, which are described below.

The Eveready microbattery [9,10], claimed to be first commercially feasible thin-film battery, consists of a sputter-deposited TiS_2 cathode and an electrolyte film sputter-deposited from a target of composition 6 Li - 4 Li_3PO_4 - P_2S_5 with either glass, mylar, alumina or paper as substrate and chromium current collectors/contacts. A film of LiI is required to provide the interfacial stability between the glassy electrolyte and lithium or TiS_2. Excellent performance has been reported from this microbattery with a maximum power density of 200 $\mu W/cm^2$, cycle life of 5-10 thousands cycles, wide range of operating temperatures (-10 to 90^0 C) and good calendar life of over 3 years

Bates [11,13] et al. at Oak Ridge National Laboratory (ORNL) utilized films deposited by sputtering Li_3PO_4 in pure N_2 (composition: $Li_{2.9}PO_{3.3}N_{0.5}$) as electrolyte, which has a conductivity of 10^{-6} S/cm. Unlike the Eveready electrolyte, this electrolyte (called LIPON) is stable with Li, thus negating the need for a protective layer of LiI. The electrolyte was initially tested with amorphous V_2O_5 cathode films deposited by sputtering a V target in Ar-O_2 mixture. The cells showed a high specific capacity of 400 mAh/g and low capacity fade during cycling of 0.034 to 0.1 % over 1200 cycles. However, the cells had high polarization and low power densities due to slow diffusion of Li (10^{-15} to 10^{-12} cm^2/s). Some preliminary studies were recently made with the spinel Mn_2O_4 cathode, e-beam evaporated and subsequently annealed at 700-800^0 C. The Li-Mn_2O_4 microbatteries showed 100 times lower resistance than the corresponding V_2O_5 cell and a low capacity fading of 0.006 % per cycle over 500 cycles. Recent studies with lithium cobalt oxide cathodes are particularly impressive for their lower cell resistance (4-5 times lower than manganese

oxides) and long cycle life (20-30 thousand cycles).

The Bellcore Li microbattery [14] consists of spinel Mn_2O_4 cathode and lithium borophosphate (LiBP) and lithium phosphorous oxynitride (LiPON) electrolyte films. The latter films were obtained differently from Bates et al., by e-beam evaporation of mixtures of B_2O_3:$LiNO_3$:Li_3PO_4. One of the challenges in depositing $LiMn_2O_4$ films was to achieve the deposition at low temperatures (< 400^0 for Ga-As and 600 ^{0} C for Si) for the substrate to be unaffected. Bellcore recently reported fabrication of such films of smaller grain size at low temperatures (< 400^0 C) through e-beam evaporation and in-situ anneal in oxygen [15]. These films yielded as little as 40 mV polarization at 200 $\mu A/cm^2$ in liquid electrolytes for over 200 cycles.

In summary, the Li microbatteries, especially those developed at ORNL, have reportedly performed well both in terms of coulombic yield, specific energy, power density and cycle life. There are, however, some processibility issues that limit the manufacturability of this technology. These include relatively slow rates of deposition of cathode/electrolyte films and post-deposition of high-temperature annealing of the cathode/electrolyte films. Furthermore, a proper methodology for integration of the thin film batteries with microelectronic devices in the same substrate needs to be established. In particular metallic substances like Li, can severely contaminate the Si substrate and drastically affect the performance of the CMOS circuits. Hence, development of a proper barrier layer may be necessary before the micro batteries can be completely integrated with the microelectronic devices.

HIGH VOLTAGE TRANSISTORS FOR AN INTEGRATED POWER MANGEMENT SYSTEM

Radiation hardness requirement for space rated integrated circuits limits the choice of usable technologies for fabrication to SOI CMOS processes [18]. Unfortunately traditional SOI CMOS technologies only support low voltage transistors in their suite of devices. Adding high voltage transistors with optimum performance parameters to the SOI CMOS process requires additional process steps. It is possible, however, to create lateral high voltage transistors in the SOI CMOS process without any changes to the fabrication sequence.

Fig. 5 shows a cross section of such a high voltage MOSFET in an SOI CMOS process. Compared to traditional low voltage devices (shown in Fig. 4), a drift region made of lightly doped material is added to the drain terminal to sustain the high voltage. This drift region is made of lightly doped junctions that already exist in the SOI CMOS process. To make high voltage NMOS transistors, the N-well junction is used as a drift channel while high voltage PMOS transistors are made by using the P-well junction as the drift channel.

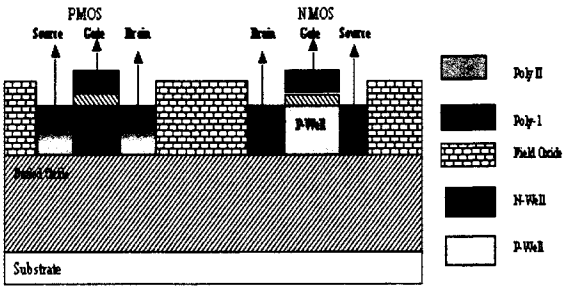

Fig. 4: Cross sections of low voltage MOSFETs in SOI CMOS technology.

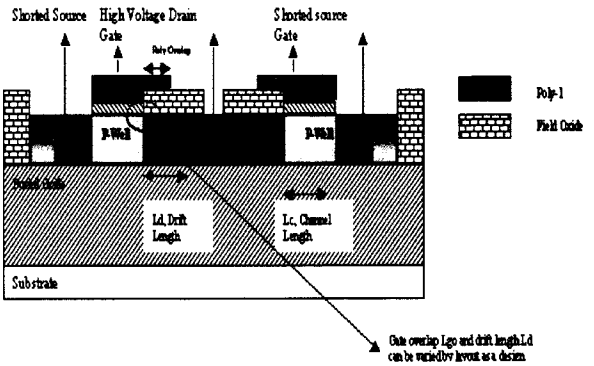

Fig. 5: Cross sections of high voltage MOSFETs in SOI CMOS technology.

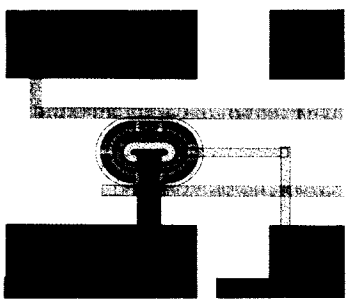

Fig. 6: Layout example of high voltage MOSFETs in SOI CMOS technology.

SOI CMOS compatible high voltage transistors can achieve voltages as high as 90V

[19]. Fig. 6 shows the layout of the high voltage MOSFET. Compared to the traditional self-aligned transistors, these devices have two additional design parameters in their layout. These parameters are the channel drift length and the drift overlap under the gate (specified in figure 5), The channel drift length and the drift overlap under the thin gate oxide influences the threshold voltage, the drain breakdown voltage and the on-resistance of the transistors [20]. The influence of these parameters on the electrical parameters of the SOI CMOS compatible transistors can be empirically characterized and the layout of the devices can be adjusted for achieving optimum performance.

One drawback of the SOI CMOS compatible transistors is that they are non-self aligned. As a result their mismatch must be considered in the design of mixed signal circuits. The second limitation of these devices is that the high voltage is only sustained between the drain and source terminals. The gate-to-source terminals on these transistors can only sustain low voltages. Finally, each transistor has a parasitic back gate that can turn on for mixed voltage applications operating at voltages higher than the threshold voltage of the parasitic back channel transistors [24,25,36]. These factors limit the use of these transistors in traditional mixed signal circuits. The need for on-chip integration of high voltage functions in rad hard SOI CMOS technologies however is motivating integrated circuit designers to develop new circuit topologies that can tolerate the performance limitations of the CMOS compatible high voltage transistors [21].

A SPACE RATED MIXED VOLTAGE MIXED SIGNAL CELL LIBRARY FOR PMAD

Fig. 7 shows a possible circuit for switching DC-DC converters for an integrated power management system. This converter uses pulse width modulation switching circuits shown in Fig. 8 and requires a complex library of mixed-signal functions. Table 2 lists the typical cells that are part of this library. The low voltage functions include a precision voltage reference and an error-correcting amplifier. The high voltage functions include a zero crossing detector, switching inductor drivers with high voltage flyback control, high voltage rectifier, high voltage regulator, and high voltage to low voltage level translator feedback.

The cells of this library will have multiple usage. For example the reference generator and the amplifiers can be used for other analog applications and the high voltage circuits can also be used as a piezo electric driver for the vibrating sensors. Additional mixed-signal circuits include a battery sensor and power loss and power up detectors.

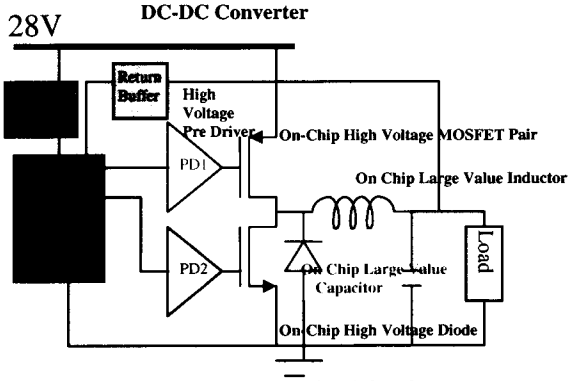

Fig. 7: A DC-DC converter for SOAC.

Most of above cells are constructed from primitive elements. These elements include differential input pair, current mirrors, single-ended gain stage and output buffer stage, and a bandgap voltage reference. Surprisingly, the circuit topologies used for these primitives are relatively independent of the chosen process (i.e., bulk CMOS vs. SOI CMOS). However there are several limitations in the performance of the SOI mixed-signal primitives. For example the input offset voltage in a single stage differential amplifier is much higher in the SOI CMOS process due to mismatch of the input transistors. A current mirror also suffers from the mismatch of the transistors and could also suffer an additional offset due to thermal gradient [27]. Finally, a traditionally designed bandgap reference generator primitive develops a large output offset due to the mismatch of the bipolar elements. To enhance the performance of the SOI CMOS primitives and compensate for the large offset between the elements, several techniques are suggested [22,23,28-32]. Techniques such as dynamic element matching and active offset cancellation, however, complicate the design.

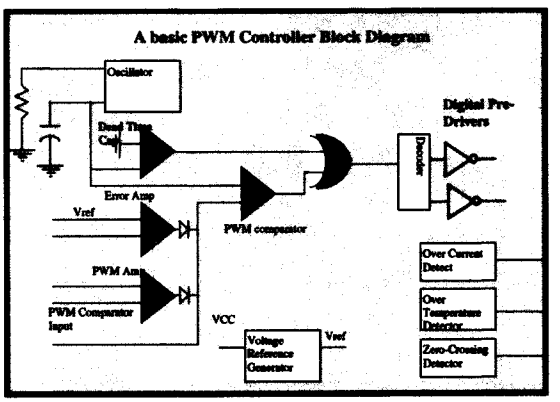

Fig. 8: Block diagram of the PWM engine.

For certain applications, however, the unique isolation features of the SOI CMOS process allows circuits that are normally available only in discrete form and not easily realizable in bulk CMOS to be fabricated. For example, a simple diode based bridge rectifier can be directly designed in the SOI CMOS technology because of the trench isolation. The trench isolation creates a natural shield that isolates the high voltage circuits from the rest of the mixed signal blocks and eliminates the need for additional shielding [20].

Table 2: Typical set of library cells for DC-DC converters.

Cell Type	
Low Voltage	Precision References
Low Voltage	High-Speed Differential Input Amplifiers
Low Voltage	Comparators
Low Voltage	Operational Amplifiers
Low Voltage	Analog Buffers
Low Voltage	Oscillators
Low Voltage	Phase/Frequency Detectors
High Voltage	Rectifiers
High Voltage	Switching Inductor Drivers
High Voltage	Voltage Regulator
High Voltage	Analog Level Translator
High Voltage	Zero Crossing Detector
High Voltage	High Side Gate Pre-Driver (PD1 in Fig. 7)

SUMMARY AND CONCLUSION

Using a combination of innovative design, advanced processing techniques and materials development, on-chip power management and distribution may be envisioned. Enabling technologies include the development of high voltage transistors compatible with SOI CMOS processes, on-chip passive components, and even on-chip back-up batteries. Such an approach will enable the development of highly functional micro/nano spacecraft by requiring less of the mass/volume budget to be dedicated to power electronics. It will also enable new, more efficient power architectures to be implemented, such as distributed adaptive PMAD.

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